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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,612	10/17/2003	Jochen Beintner	FIS920020080US2	2444

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/688,612	BEINTNER ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/17/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 12 is objected to because of the following informalities: In line 2 the examiner believes "is" should be replaced with – in-- to fix a typographical error. Appropriate correction is required.

Claim 14 is objected to because of the following informalities: In line 4 the examiner believes "300 B 1000 W" should be replaced with – between 300 to 1000 W-- to fix a typographical error. Appropriate correction is required.

Claim 18 is objected to because of the following informalities: In line 2 the examiner believes "is" should be replaced with – in-- to fix a typographical error. Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 12, 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Mandelman et al. (U.S. Patent No. 6,455,886).

In re claim 12, Mandelman et al. ('886) discloses the method of forming a memory device, said method comprising:

patterning a trench in a substrate (see column 4, lines 49-56 and Figure 3);

filling a lower portion of said trench with a capacitor conductor (108);

forming a doped trench top oxide (112) in said trench above said capacitor conductor; and

heating said structure to form a conductive buried strap in said substrate adjacent said trench top oxide (see column 6, lines 5-20).

In re claim 16, Mandelman et al. ('886) discloses the method further comprising depositing an undoped trench top oxide layer (116) in said trench above said doped trench top oxide.

In re claim 17, Mandelman et al. ('886) discloses further comprising depositing a gate conductor (120) in said trench above said undoped trench top oxide layer, wherein said undoped trench top oxide layer insulates said gate conductor from said capacitor conductor.

In re claim 18, Mandelman et al. ('886) discloses a method of forming a memory device said method comprising:

patterning a trench in a substrate (see column 4, lines 49-56 and Figure 3);

filling a lower portion of said trench with a capacitor conductor (108); and

forming a trench top oxide (112, 116) in said trench above said capacitor conductor, wherein said forming of s said trench top oxide includes depositing a doped trench top oxide layer above said capacitor conductor, and forming an undoped trench top oxide layer above said doped trench top oxide layer.

In re claim 19, Mandelman et al. ('886) discloses the method further comprising depositing a conductive node strap (110) in said trench adjacent said capacitor conductor.

In re claim 20, Mandelman et al. ('886) disclose the method further comprising heating said structure to form a conductive buried strap in said substrate adjacent said trench top oxide (see column 5, lines 60 through column 6, lines 21).

Claims 12, 16-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Mandelman et al. (U.S. Patent No. 6,555,862).

In re claim 12, Mandelman et al. ('862) discloses the method of forming a memory device, said method comprising:

patterning a trench in a substrate (102);

filling a lower portion of said trench with a capacitor conductor (110);

forming a doped trench top oxide (120) in said trench above said capacitor conductor; and

heating said structure to form a conductive buried strap in said substrate adjacent said trench top oxide (see column 5, lines 9-26).

In re claim 16, Mandelman et al. ('862) discloses the method further comprising depositing an undoped trench top oxide layer (122) in said trench above said doped trench top oxide.

In re claim 17, Mandelman et al. ('862) discloses further comprising depositing a gate conductor (142) in said trench above said undoped trench top oxide layer, wherein

said undoped trench top oxide layer insulates said gate conductor from said capacitor conductor.

In re claim 18, Mandelman et al. ('862) discloses a method of forming a memory device said method comprising:

patterning a trench in a substrate (102);

filling a lower portion of said trench with a capacitor conductor (110); and

forming a trench top oxide (120, 122) in said trench above said capacitor conductor, wherein said forming of s said trench top oxide includes depositing a doped trench top oxide layer above said capacitor conductor, and forming an undoped trench top oxide layer above said doped trench top oxide layer.

In re claim 19, Mandelman et al. ('862) discloses the method further comprising depositing a conductive node strap (112) in said trench adjacent said capacitor conductor.

In re claim 20, Mandelman et al. ('862) disclose the method further comprising heating said structure to form a conductive buried strap in said substrate adjacent said trench top oxide (see column 5, lines 9-26).

Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Chang et al. (U.S. Patent No. 6,696,717).

In re claim 12, Chang et al. discloses the method of forming a memory device, said method comprising:

patterning a trench in a substrate (see column 2, lines 35-55);

filling a lower portion of said trench with a capacitor conductor (104);

forming a doped trench top oxide (ASG, see column 2 line 64 through column 3 line 3) in said trench above said capacitor conductor; and

heating said structure to form a conductive buried strap in said substrate adjacent said trench top oxide (see column 2 line 64 through column 3 line 3).

Claims 18-19 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Divakaruni et al. (U.S. Patent No. 6,420,750).

In re claim 18, Divakaruni et al discloses a method of forming a memory device said method comprising:

patterning a trench in a substrate (24);

filling a lower portion of said trench with a capacitor conductor (20); and

forming a trench top oxide (40, 60, see column 3, line 50 through column 4 line 20) in said trench above said capacitor conductor, wherein said forming of s said trench top oxide includes depositing a doped trench top oxide layer above said capacitor conductor, and forming an undoped trench top oxide layer above said doped trench top oxide layer.

In re claim 19, Divakaruni et al. discloses the method further comprising depositing a conductive node strap (100) in said trench adjacent said capacitor conductor.

In re claim 21, Divakaruni et al. discloses the method wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-CVD) process (see column 3, line 55 through column 4, line 10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-15 and 21 –22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (U.S. Patent No. 6,455,886) in view of M'Saad (U.S. Patent No. 6,013,584).

Mandelman ('886) et al. discloses the method as claimed and rejected above, but does not disclose the method wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-CVD) process, wherein said process of depositing said doped trench top oxide comprises the following parameters: depositing rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000 W, and a phosphine gas delivery at gas flows below 5 sccm and wherein during said process of depositing said doped trench top oxide layer, a percentage by weight of dopants in aid duped trench top oxide layer is less than 1%.

M'Saad discloses the method wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-

CVD) process, wherein said process of depositing said doped trench top oxide comprises the following parameters: depositing rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000W (see column 11, lines 8-28), and a phosphine gas delivery at gas flows below 5 sccm (see column 10, lines 15-60). The examiner notes as M'Saad discloses the flow rate of phosphine to be 10% of the flowrate of the silane, which may be 30- 50 sccm, means that phosphine is disclosed to have a flow rate less than 5 sccm.

M'Saad also discloses the method of forming the PSG film with less than 1% by weight of dopant (see column 11, lines 40-45). The examiner notes that Applicants teach that by forming the doped layer with the above parameters of the rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000W, and a phosphine gas delivery at gas flows below 5 sccm forms a film with a dopant concentration less than 1%. Therefore, the examiner asserts that the method of M'Saad during said process of depositing said doped trench top oxide layer, a percentage by weight of dopants in said doped trench top oxide layer will be less than 1%.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer of Mandelman et al. ('886) by the method of M'Saad because as M'Saad teaches the method allows for a dielectric layer with low moisture content and good gap fill capability (see abstract, M'Saad)

Claims 13-15 and 21 –22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. (U.S. Patent No. 6,555,862) in view of M'Saad (U.S. Patent No. 6,013,584).

Mandelman ('862) et al. discloses the method as claimed and rejected above, but does not disclose the method wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-CVD) process, wherein said process of depositing said doped trench top oxide comprises the following parameters: depositing rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000 W, and a phosphine gas delivery at gas flows below 5 sccm and wherein during said process of depositing said doped trench top oxide layer, a percentage by weight of dopants in aid duped trench top oxide layer is less than 1%.

M'Saad discloses the method wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-CVD) process, wherein said process of depositing said doped trench top oxide comprises the following parameters: depositing rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000W (see column 11, lines 8-28), and a phosphine gas delivery at gas flows below 5 sccm (see column 10, lines 15-60). The examiner notes as M'Saad discloses the flow rate of phosphine to be 10% of the flowrate of the silane, which may be 30- 50 sccm, means that phosphine is disclosed to have a flow rate less than 5 sccm.

M'Saad also discloses the method of forming the PSG film with less than 1% by weight of dopant (see column 11, lines 40-45). The examiner notes that Applicants

teach that by forming the doped layer with the above parameters of the rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000W, and a phosphine gas delivery at gas flows below 5 sccm forms a film with a dopant concentration less than 1%. Therefore, the examiner asserts that the method of M'Saad during said process of depositing said doped trench top oxide layer, a percentage by weight of dopants in said doped trench top oxide layer will be less than 1%.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer of Mandelman et al. ('862) by the method of M'Saad because as M'Saad teaches the method allows for a dielectric layer with low moisture content and good gap fill capability (see abstract, M'Saad)

Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,696,717) in view of M'Saad (U.S. Patent No. 6,013,584).

Chang et al. discloses the method as claimed and rejected above, but does not disclose the method wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-CVD) process, wherein said process of depositing said doped trench top oxide comprises the following parameters: depositing rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000 W, and a phosphine gas delivery at gas flows below 5

sccm and wherein during said process of depositing said doped trench top oxide layer, a percentage by weight of dopants in aid duped trench top oxide layer is less than 1%.

M'Saad discloses the method wherein said process of depositing said doped trench top oxide comprises a high density plasma-chemical vapor deposition (HDP-CVD) process, wherein said process of depositing said doped trench top oxide comprises the following parameters: depositing rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000W (see column 11, lines 8-28), and a phosphine gas delivery at gas flows below 5 sccm (see column 10, lines 15-60). The examiner notes as M'Saad discloses the flow rate of phosphine to be 10% of the flowrate of the silane, which may be 30- 50 sccm, means that phosphine is disclosed to have a flow rate less than 5 sccm.

M'Saad also discloses the method of forming the PSG film with less than 1% by weight of dopant (see column 11, lines 40-45). The examiner notes that Applicants teach that by forming the doped layer with the above parameters of the rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000W, and a phosphine gas delivery at gas flows below 5 sccm forms a film with a dopant concentration less than 1%. Therefore, the examiner asserts that the method of M'Saad during said process of depositing said doped trench top oxide layer, a percentage by weight of dopants in said doped trench top oxide layer will be less than 1%.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer of Chang et al. by the method of

M'Saad because as M'Saad teaches the method allows for a dielectric layer with low moisture content and good gap fill capability (see abstract, M'Saad)

Claim 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Divakaruni et al. (U.S. Patent No. 6,420,750) in view of M'Saad (U.S. Patent No. 6,013,584).

Divakaruni et al. discloses the method as claimed and rejected above, but does not disclose the method wherein during said process of depositing said doped trench top oxide layer, a percentage by weight of dopants in aid duped trench top oxide layer is less than 1%.

M'Saad discloses the method of forming the PSG film with less than 1% by weight of dopant (see column 11, lines 40-45). The examiner notes that Applicants teach that by forming the doped layer with the above parameters of the rate of silane reactant gas flow 10-75 sccm, approximate bias plasma power between 300-1000W, and a phosphine gas delivery at gas flows below 5 sccm forms a film with a dopant concentration less than 1%. Therefore, the examiner asserts that the method of M'Saad during said process of depositing said doped trench top oxide layer, a percentage by weight of dopants in said doped trench top oxide layer will be less than 1%.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the doped oxide layer of Chang et al. by the method of

M'Saad because as M'Saad teaches the method allows for a dielectric layer with low moisture content and good gap fill capability (see abstract, M'Saad)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812

jmk